Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	((re$1order$4 adj commands) and ((array adj controller) near4 sequencers) and (penalty adj box) and expire).clm.	US-PGPUB	OR	ON	2005/11/18 14:25

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	2864	re$1order$4 near3 ("commands" or "transactions" or "requests")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 13:39
L3	17946	(penal$5 or delay$4) with command	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 13:33
L4	908	bank with conflict$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 13:34
L5	6	2 and 3 and 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 14:01
L8	95	("5822772" "6052772" "6628292" "6633298" "6088772" "6092158" "6711055" "6751712" "4949245" "5555390" "5930820" "5822251" "6182192" "6195306" "4342079" "5264742" "5522061" "5600605" "5627791" "5629513" "5636173" "5713011" "5748551" "5790468" "5903509" "5910181" "5999197" "6097404" "6108265" "6151273" "6157990" "6192446" "6226755" "6226755" "6282638" "6288728" "6295231" "6340973" "6356505" "6370640" "6418077" "6466221" "6556506" "6754126" "6098155" "5220545" "5504900" "5974571" "6055598" "5606679").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 13:38
L9	0	5 and 8	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 13:37
L10	71	penalty adj box	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 13:39

L11	2	2 and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 13:39
L12	10	re$1order$4 and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 13:39
L13	6208	(711/158, 711/5, 711/105, 711/150, 711/151, 711/154, 711/167, 711/168).ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 14:10
L14	170	13 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 14:10
L15	5	13 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/18 14:10

Terms used
reordering sentence commands or **transactions** or **requests** and **penalty** or **delay** and **bank conflict**

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1 Concurrency, latency, or system overhead: which has the largest impact on uniprocessor DRAM-system performance?

Vinodh Cuppu, Bruce Jacob

May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture ISCA '01**, Volume 29 Issue 2

Publisher: ACM Press

Full text available: pdf(904.17 KB) Additional Information: full citation, abstract, references, citings, index terms

Given a fixed CPU architecture and a fixed DRAM timing specification, there is still a large design space for a DRAM system organization. Parameters include the number of memory channels, the bandwidth of each channel, burst sizes, queue sizes and organizations, turnaround overhead, memory-controller page protocol, algorithms for assigning request priorities and scheduling requests dynamically, etc. In this design space, we see a wide variation in application execution times: for example, ...

2 Special issue: AI in engineering

D. Sriram, R. Joobbani

April 1985 **ACM SIGART Bulletin**, Issue 92

Publisher: ACM Press

Full text available: pdf(8.79 MB) Additional Information: full citation, abstract

The papers in this special issue were compiled from responses to the announcement in the July 1984 issue of the SIGART newsletter and notices posted over the ARPAnet. The interest being shown in this area is reflected in the sixty papers received from over six countries. About half the papers were received over the computer network.

3 Illustrative risks to the public in the use of computer systems and related technology

Peter G. Neumann

January 1992 **ACM SIGSOFT Software Engineering Notes**, Volume 17 Issue 1

Publisher: ACM Press

Full text available: pdf(1.65 MB) Additional Information: full citation, citings, index terms

4 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli
April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2
Publisher: ACM Press

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

5 Distributed operating systems
Andrew S. Tanenbaum, Robbert Van Renesse
December 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 4
Publisher: ACM Press

Full text available: pdf(5.49 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Distributed operating systems have many aspects in common with centralized ones, but they also differ in certain ways. This paper is intended as an introduction to distributed operating systems, and especially to current university research about them. After a discussion of what constitutes a distributed operating system and how it is distinguished from a computer network, various key design issues are discussed. Then several examples of current research projects are examined in some detail ...

6 Hardware-only stream prefetching and dynamic access ordering
Chengqiang Zhang, Sally A. McKee
May 2000 **Proceedings of the 14th international conference on Supercomputing**
Publisher: ACM Press

Full text available: pdf(1.06 MB) Additional Information: full citation, abstract, references, citings, index terms

Memory system bottlenecks limit performance for many applications, and computations with strided access patterns are among the hardest hit. The streams used in such applications have extremely poor cache behavior. These access patterns have the advantage of being predictable, though, and this can be exploited to improve the efficiency of the memory subsystem in two ways: memory latencies can be masked by prefetching stream data, and the latencies can be reduced by reordering stream accesses ...

7 Illustrative risks to the public in the use of computer systems and related technology
Peter G. Neumann
January 1996 **ACM SIGSOFT Software Engineering Notes**, Volume 21 Issue 1
Publisher: ACM Press

Full text available: pdf(2.54 MB) Additional Information: full citation

8 Continuous program optimization: A case study
Thomas Kistler, Michael Franz
July 2003 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 25 Issue 4
Publisher: ACM Press

Full text available: pdf(877.67 KB) Additional Information: full citation, abstract, references, index terms, review

Much of the software in everyday operation is not making optimal use of the hardware on which it actually runs. Among the reasons for this discrepancy are hardware/software mismatches, modularization overheads introduced by software engineering considerations, and the inability of systems to adapt to users' behaviors.A solution to these problems is to delay code generation until load time. This is the earliest point at which a piece of software can be fine-tuned to the actual capabilities of the ...

Keywords: Dynamic code generation, continuous program optimization, dynamic reoptimization

9 Relief from the audio interface blues: expanding the spectrum of menu, list, and form styles

Paul Resnick, Robert A. Virzi
June 1995 **ACM Transactions on Computer-Human Interaction (TOCHI)**, Volume 2 Issue 2
Publisher: ACM Press

Full text available: pdf(2.13 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Menus, lists, and forms are the workhorse dialogue structures in telephone-based interactive voice response applications. Despite diversity in applications, there is a surprising homogeneity in the menu, list, and form styles commonly employed. There are, however, many alternatives, and no single style fits every prospective application and user population. A design space for each dialogue structure organizes the alternatives and provides a framework for analyzing their benefits and drawbac ...

Keywords: ADSI, PDA, forms, interactive voice response, menus, skip and scan, voice mail

10 A performance comparison of contemporary DRAM architectures

Vinodh Cuppu, Bruce Jacob, Brian Davis, Trevor Mudge
May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture ISCA '99**, Volume 27 Issue 2
Publisher: IEEE Computer Society, ACM Press

Full text available: pdf(166.88 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In response to the growing gap between memory access time and processor speed, DRAM manufacturers have created several new DRAM architectures. This paper presents a simulation-based performance study of a representative group, each evaluated in a small system organization. These small-system organizations correspond to workstation-class computers and use on the order of 10 DRAM chips. The study covers Fast Page Mode, Extended Data Out, Synchronous, Enhanced Synchronous, Synchronous Link, Rambus, ...

11 On automated message processing in electronic commerce and work support systems: speech act theory and expressive felicity

Steven O. Kimbrough, Scott A. Moore
October 1997 **ACM Transactions on Information Systems (TOIS)**, Volume 15 Issue 4
Publisher: ACM Press

Full text available: pdf(502.20 KB) Additional Information: full citation, abstract, references, citings, index terms

Electronic messaging, whether in an office environment or for electronic commerce, is normally carried out in natural language, even when supported by information systems. For a variety of reasons, it would be useful if electronic messaging systems could have

semantic access to, that is, access to the meanings and contents of, the messages they process. Given that natural language understanding is not a practicable alternative, there remain three approaches to delivering systems with semant ...

Keywords: electronic commerce, formal language for business communication, speech act theory

12 Experience with a software-defined machine architecture

David W. Wall

May 1992 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 14 Issue 3

Publisher: ACM Press

Full text available: pdf(2.66 MB) Additional Information: full citation, abstract, references, citings, index terms, review

We have built a system in which the compiler back end and the linker work together to present an abstract machine at a considerably higher level than the actual machine. The intermediate language translated by the back end is the target language of all high-level compilers and is also the only assembly language generally available. This lets us do intermodule register allocation, which would be harder if some of the code in the program had come from a traditional assembler, out of sight of ...

Keywords: RISC, graph coloring, intermediate language, interprocedural, optimization, pipeline scheduling, profiling, register allocation, register windows

13 Interleaved parallel schemes: improving memory throughput on supercomputers

André Seznec, Jacques Lenfant

April 1992 **ACM SIGARCH Computer Architecture News , Proceedings of the 19th annual international symposium on Computer architecture ISCA '92**, Volume 20 Issue 2

Publisher: ACM Press

Full text available: pdf(922.60 KB) Additional Information: full citation, abstract, references, citings, index terms

On many commercial supercomputers, several vector register processors share a global highly interleaved memory in a MIMD mode. When all the processors are working on a single vector loop, a significant part of the potential memory throughput may be wasted due to the asynchronism of the processors. In order to limit this loss of memory throughput, a SIMD synchronization mode for vector accesses to memory may be used. But an important part of the memory bandwidth may be wasted when ...

14 Data base directions: the next steps

John L. Berg

November 1976 **ACM SIGMOD Record , ACM SIGMIS Database**, Volume 8 , 8 Issue 4 , 2

Publisher: ACM Press

Full text available: pdf(9.95 MB) Additional Information: full citation, abstract

What information about data base technology does a manager need to make prudent decisions about using this new technology? To provide this information the National Bureau of Standards and the Association for Computing Machinery established a workshop of approximately 80 experts in five major subject areas. The five subject areas were auditing, evolving technology, government regulations, standards, and user experience. Each area prepared a report contained in these proceedings. The proceedings p ...

Keywords: DBMS, auditing, cost/benefit analysis, data base, data base management, government regulation, management objectives, privacy, security, standards, technology

assessment, user experience

15 Document Formatting Systems: Survey, Concepts, and Issues

Richard Furuta, Jeffrey Scofield, Alan Shaw
September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3
Publisher: ACM Press
Full text available: pdf(5.36 MB) Additional Information: full citation, references, citings, index terms

16 Risks to the public

P. G. Neumann
October 1987 **ACM SIGSOFT Software Engineering Notes**, Volume 12 Issue 4
Publisher: ACM Press
Full text available: pdf(1.60 MB) Additional Information: full citation, index terms

17 Combining optimism and pessimism to produce high availability in distributed transaction processing

Joel M. Crichlow
July 1994 **ACM SIGOPS Operating Systems Review**, Volume 28 Issue 3
Publisher: ACM Press
Full text available: pdf(832.79 KB) Additional Information: full citation, abstract, index terms

In a distributed system some or all of the data items are replicated and stored at separate nodes. This increases the availability of these items and it is then possible to complete transactions faster than in single node systems. Hovever the concurrent processing of transactions at separate nodes can generate inconsistencies in the stored information. Some mechanism must be employed to address the inconsistencies that can arise. A system has been designed that allows a transaction to be process ...

18 Risks to the public: Risks to the public in computers and related systems

Peter G. Neumann
May 2002 **ACM SIGSOFT Software Engineering Notes**, Volume 27 Issue 3
Publisher: ACM Press
Full text available: pdf(1.92 MB) Additional Information: full citation

19 Memory aware compilation through accurate timing extraction

Peter Grun, Nikil Dutt, Alex Nicolau
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(79.24 KB) Additional Information: full citation, abstract, references, citings, index terms

Memory delays represent a major bottleneck in embedded systems performance. Newer memory modules exhibiting efficient access modes (e.g., page-, burst-mode) partly alleviate this bottleneck. However, such features can not be efficiently exploited in processor-based embedded systems without memory-aware compiler support. We describe a memory-aware compiler approach that exploits such efficient memory access modes by extracting accurate timing information, allowing the compiler's sche ...

20

DCD—disk caching disk: a new approach for boosting I/O performance

Yiming Hu, Qing Yang

May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2

Publisher: ACM Press

Full text available: pdf(1.29 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a novel disk storage architecture called *DCD,* Disk Caching Disk, for the purpose of optimizing I/O performance. The main idea of the *DCD* is to use a small log disk, referred to as *cache-disk,* as a secondary disk cache to optimize write performance. While the cache-disk and the normal data disk have the same physical properties, the access speed of the former differs dramatically from the latter because of different data units and different ways in which d ...

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